REMARKS

This paper is in response to the Office Action of March 6, 2007. Claims 1-3, 5-7, 9, and 21-24 are pending in this application. Applicants have amended the application as set forth above. Specifically, Claim 1 has been amended. No new matter is added by the amendment as discussed below. Applicants respectfully request the entry of the amendment and reconsideration of the application in view of the above amendment and the following remarks.

Discussion of Amendment

The amendments to Claim 1 are made to add "providing an insulation layer having a damascene trench therein on a substrate, the damascene trench including sidewalls" to Claim 1. In addition, Claim 1 has been amended to recite that a barrier layer is formed *directly on surfaces of the insulation layer including the sidewalls within the damascene trench*. The amendments to Claim 1 are also made to clarify that a copper layer is formed *directly on the barrier layer such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*.

Support for the amendment to Claim 1 can be found in, for example, Figures 2A and 3 and paragraphs 0012, 0013, 0021, 0022, and 0030 of Patent Application Publication No. 2005/0124154 of the subject application. Specifically, paragraph 0012 supports providing an insulation layer having a damascene trench therein by stating that "According to the present invention, a method for forming high reliability copper interconnecting conductors connecting high density semiconductor circuits on *an insulation layer in which a damascene structure is pre-formed on a substrate* by forming a barrier layer, a adhesion layer or both, where such layers have a high quality adhesion characteristics with a copper layer, is disclosed." Paragraph 0021 supports the insulation layer having trenches. In addition, paragraphs 0013 and 0022 and FIG. 2A in combination describe that the barrier layer is formed *directly on surfaces of the insulation layer including the sidewalls within the damascene trench*. Paragraph 0013 supports that the copper layer is formed *directly* on the barrier layer *such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*.

As such, Applicants respectfully submit that the amendments to Claim 1 are fully supported by the application as originally filed and does not constitute the addition of new matter. Therefore,

Applicants respectfully request the entry of the amendments.

Rejection Under 35 U.S.C. § 103

The Examiner rejected Claims 1, 6, and 7 under 35 U.S.C. 103(a) as being unpatentable over Kirlin et al. (U.S. Patent No. 6,320,213) in combination with Soininen et al. (U.S. Patent No. 6,482,740). Claims 2, 3, 5, 9, and 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kirlin et al./Soininen et al. and further in view of Kim et al. (U.S. Patent No. 6,936,535), Koh et al. (U.S. Patent No. 6,720,262), and Gelatos et al. (U.S. Patent No. 5,391,517).

Standard for Obviousness Rejection

The Patent and Trademark Office has the burden under section 103 to establish a *prima facie* case of obviousness. *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-87 (Fed. Cir. 1984). To establish a *prima facie* case of obviousness, the following criteria must be met: there must be a reasonable expectation of success; and the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143.

Claims 1, 6, and 7

With respect to Claim 1 as amended, Applicants submit that the Office Action fails to establish a *prima facie* case of obviousness. Kirlin et al. and Soininen et al., individually or in combination, fail to teach or suggest all the limitations of Claim 1 as amended.

Claim 1 requires 1) providing an insulation layer having a damascene trench therein on a substrate, the damascene trench including sidewalls; 2) forming a ruthenium or rhenium barrier layer *directly on surfaces of the insulation layer including the sidewalls within the damascene trench* using an atomic layer deposition (ALD) method; and 3) forming a copper layer *directly on said barrier layer such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*. Thus, a single Ru or Re barrier layer to copper diffusion is formed to intervene between the insulation layer and the sidewalls of the damascene trench within the insulation layer. Recitation of direct formation also requires the copper to directly overlie the barrier while the barrier directly overlies the insulating trench

sidewalls.

The prior art references do not teach or suggest forming such a single Ru or Re barrier layer which intervenes between, and directly contacts, the copper layer and the sidewalls of the damascene trench within the insulation layer. Kirlin et al. only teaches or suggests forming a barrier layer which is positioned only at the bottom of a damascene trench and is interposed between a conductive electrode and a metallization layer (copper or other conductive metals), and thus fails to teach or suggest a Ru or Re barrier intervening copper and the insulating sidewalls of a damascene trench. Soininen et al. only teaches or suggests forming two layers (a metal nitride barrier layer and a Ru- or Re-containing seed layer) between an insulation layer and copper in a damascene trench, and thus fails to teach or suggest *directly* forming a Ru or Re barrier on surfaces of the insulating layer.

a. Kirlin et al.

Kirlin et al. discloses methods of making an IC circuit device having a capacitor. *See* Kirlin, column 2, lines 23-25. Kirlin et al. discloses a method of forming a metallization layer 130 which includes: forming a barrier layer 120 on a capacitor structure 110, 112, 116; forming an interlevel dielectric layer 122; forming via openings 125 (see Figure 10 of Kirlin et al.) through the dielectric layer 122; and depositing a conductive material (e.g., Al, Al alloy, W, W alloy, Cu, and Cu alloy) to fill the via openings 125. *Id.* at Figures 8-11; and column 6, line 37 to column 7, line 20. The resulting structure is shown in Figure 11 below of Kirlin et al.

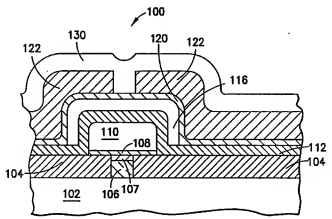

FIG.11

Kirlin et al. discloses another method of forming a metallization layer 238 which includes: forming contact plug holes 221, 222, 223 in an interlevel dielectric layer 218 (see Figure 21 of Kirlin et al.); forming a barrier layer 230 on the interlevel dielectric layer 218 (see Figure 22 of Kirlin et al.); etching the barrier layer 230 to leave portions 232, 234, 236 of the barrier layer 230 only at the bottom of the contact plug holes 221, 222, 223 (each of the portions contacts one of the capacitor electrodes 212, 216 or the substrate 202); and depositing a conductive material (e.g., Pt, Al, Al alloy, W, and W alloy) on the interlevel dielectric layer 218 and the remaining portions 232, 234, 236 of the barrier layer 230 (see Figure 24 of Kirlin below). *Id.* at Figures 21-24; and column 8, line 55 to column 9, line 55.

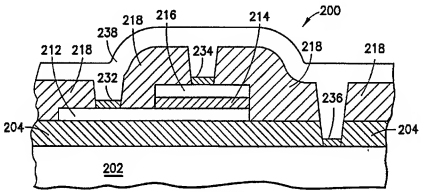

FIG.24

b. Soininen et al.

Soininen et al. discloses a dual damascene structure. Soininen et al., Figure 1 below. The dual damascene structure consists of a metallization layer 2, e.g., Cu, an insulating layer 4, e.g., SiO_2, a via etch stop 6 made of, e.g., Si_3N_4, a via level insulator 8, e.g., SiO_2, a trench etch stop 10 made of, e.g., Si_3N_4, a trench level insulator 12, e.g., SiO_2, a diffusion barrier 14, e.g., TaN, a seed layer 16 (e.g., metal oxides such as ReO_2 and RuO_2) and a via/trench fill metal 18, e.g., Cu. *See id.* at Figure 1; column 5, lines 46-52; column 6, lines 43-53; and column 7, lines 21-37.

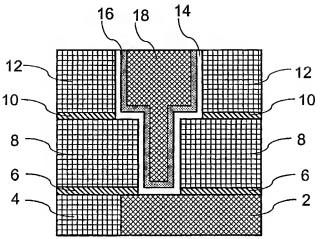

Fig. 1

Soininen et al. also discloses forming a Ru or Re layer by an ALD type process. *Id.* at column 5, lines 5-25. In addition, Soininen et al. discloses depositing copper on a diffusion barrier layer using a CVD process. *Id.* at column 3, lines 15-35. As indicated in the Office Action, Soininen et al. does not disclose forming a Ru or Re layer directly on an insulating layer.

c. Claim 1 v. Combinations of Kirlin and Soininen

Claim 1 of the present application is directed to a method for forming copper interconnection conductors for interconnecting integrated circuits on a substrate. Claim 1 as amended requires 1) providing an insulation layer having a damascene trench therein on a substrate, the damascene trench including sidewalls; 2) forming a barrier layer using ruthenium (Ru) or rhenium (Re) or their alloys *directly on surfaces of the insulation layer including the sidewalls within the damascene trench* using an atomic layer deposition (ALD) method; and 3) forming a copper layer *directly* on said barrier layer using chemical vapor deposition (CVD) *such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer.*

A. Claim 1 is patentable over Kirlin et al. in view of Soininen et al.

The method recited in Claim 1 as amended provides forming "forming a copper layer directly on said barrier layer *such that the barrier layer intervenes between the copper layer and*

the sidewalls of the damascene trench within the insulation layer." Kirlin et al. fails to disclose this limitation by the two methods set forth above.

In the first method (Figures 8-11) of Kirlin et al. explained above, the barrier layer 120 is formed before forming the interlevel dielectric layer 122. It should be noted that a layer 112 of high dielectric constant material is ***not*** an insulation layer *having a damascene trench therein*, as recited in Claim 1 as amended. After forming the interlevel dielectric layer 122, a portion of the barrier layer 120 is exposed through via openings 125. The metallization layer 130 (e.g., a copper layer) is then formed on the interlevel dielectric layer 122. As shown in Figure 11 of Kirlin et al., the metallization layer 130 contacts a portion of the barrier layer 120, which overlies an upper electrode formed of, for example, platinum. However, no portion of the barrier layer 120 intervenes between the metallization layer 130 and the interlevel dielectric layer 122. Therefore, Kirlin et al. fails to disclose that a copper layer is formed *such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*, as recited in Claim 1 as amended.

In the second method (Figures 21-24) of Kirlin et al., the barrier layer 230 is formed on the interlevel dielectric layer 218 having contact plug holes 221, 222, 223. However, a substantial portion of the barrier layer 230 is removed from the interlevel dielectric layer 218, leaving only portions 232, 234, 236 of the barrier layer 230 at the bottom of the contact plug holes 221, 222, 223. The metallization layer 238 formed thereafter contacts the barrier layer portions 232, 234, 236. Kirlin et al., however, only discloses that the metallization layer 238 is formed of a *non-copper metal* (e.g., Pt, Al, Al alloy, W, and W alloy) in this method. Thus, Kirlin et al. fails to disclose that a copper layer is formed directly on the barrier layer in this second method. Assuming *arguendo* that it might be obvious to replace the metallization layer with copper as in the first method, Kirlin et al. still fails to disclose "*such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*" because none of the remaining barrier layer portions 232, 234, 236 is interposed between the metallization layer 238 and the interlevel dielectric layer 218. Kirlin et al. therefore fails to disclose "forming a copper layer *directly* on said barrier layer *such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer* " with either or a combination of the two methods.

Soininen et al. does not cure this deficiency. Soininen et al. fails to disclose a single barrier layer which intervenes between and contacts both an insulation layer and a copper layer. Soininen et al. discloses forming a barrier layer 14 between a seed layer 16 and an insulation layer 8, 12. *See* Soininen et al., Figure 1; and column 5, lines 46-52. The trench fill metal (e.g., copper) 18 is not formed directly on this barrier layer 14. Soininen et al. also discloses forming a seed layer (formed of, for example, ruthenium or rhenium oxide) 16 between the trench fill metal 18 and the barrier layer 14. This seed layer 16 is not formed directly on surfaces of the insulation layer 8, 12. *See id.* Therefore, Soininen et al. does not cure the deficiency of Kirlin et al.

B. Claim 1 is patentable over Soininen et al. in view of Kirlin et al.

The Examiner states on page 4 of the Office Action that "Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Soininen et al. with the diffusion barrier layer of ruthenium or ruthenium alloys formed directly on the surface of the insulation layer because *ruthenium or ruthenium alloys are compatible materials that can be used to substitute nitride barrier layer* as recognized by Kirlin et al. to have substantially no diffusion of oxygen, platinum, copper or aluminum to occur." Applicants respectfully disagree with the Examiner for the following reasons.

The damascene embodiment (Figure 1) of Soininen et al. expressly includes a metal nitride barrier layer 14 between the insulator 8, 12 and the (Ru- or Re-containing) seed layer 16. In addition, even if Ru is recognized by Kirlin et al. as a diffusion barrier, that does not give a skilled artisan any reason to form a single Ru layer which intervenes between and contacts an insulating layer and a copper layer in the context of Soininen et al. As set forth above, Kirlin et al. only discloses a barrier layer which intervenes between and contacts *a conductive electrode 116, 212, 216 (or substrate 202) and a metallization layer 130, 238.* See Figures 11 and 24 above of Kirlin et al. Thus, the skilled artisan would not be taught to ***omit or substitute*** the TaN barrier layer 14 of Soininen et al. to meet the claimed limitation.

Put another way, neither of the references recognizes Ru or Re as a suitable sole barrier *between and directly contacting* copper and the insulator in which a damascene trench is formed. Kirlin et al. does not show any barrier in that position. Soininen et al. uses both a metal nitride

layer and an Ru- or Re-containing layer in that position.

The characteristic of Ru recognized by Kirlin et al. does not suggest that Ru or Re should serve as a copper barrier directly on an insulation layer because there is no Ru or Re layer directly on the insulation layer within the dual damascene trench of Soininen et al. Kirlin et al. does not cure this deficiency because it also fails to disclose Ru formed to intervene between a damascene insulation layer and a copper layer.

Persons of ordinary skill may recognize that the Ru seed layer 16 can also serve as a barrier layer as well as a seed layer at the position shown in Figure 1 of Soininen et al. However, nothing in the art suggests omitting Soininen's metal nitride layer 14 from between the Ru 16 and the insulator 8, 12 that defines damascene trenches.

As set forth above, Kirlin et al. and Soininen et al., either individually or in combination, fail to teach or suggest all the limitations of Claim 1. Thus, the Office Action fails to establish a *prima facie* case of obviousness. Therefore, Claim 1 is allowable under 35 U.S.C. 103(a) over Kirlin et al. in combination with Soininen et al. Claims 6 and 7 depend directly or indirectly from Claim 1, and are allowable for substantially the same reasons as explained above.

Claims 2, 3, 5, 9, and 21-24

With respect to Claims 2, 3, 5, 9, and 21-24, Applicants submit that the Office Action fails to establish a *prima facie* case of obviousness. Kirlin et al., Soininen et al., Kim et al., Koh et al., and Gelatos et al., either alone or in combination, do not teach or suggest all the limitations of the claims.

Claims 2, 3, 5, 9, and 21-24 depend directly or indirectly from Claim 1. As set forth above, Kirlin et al. and Soininen et al., either individually or in combination, fail to teach or suggest all the limitations of Claim 1. Kim et al., Koh et al., and Gelatos et al., either individually or in combination, fail to cure this deficiency. None of these three references teaches or suggests "forming a copper layer *directly on said barrier layer such that the barrier layer intervenes between the copper layer and the sidewalls of the damascene trench within the insulation layer*," as recited in Claim 1 as amended. Therefore, Claims 2, 3, 5, 9, and 21-24 are allowable under 35 U.S.C. 103(a) over the combination of Kirlin et al./Soininen et al. and further in view of Kim et

al., Koh et al., and Gelatos et al.

For all of these reasons, Applicants respectfully request withdrawal of this rejection, and allowance of the pending claims.

CONCLUSION

In view of Applicants' amendments to the claims and the foregoing remarks, Applicants respectfully submit that the present application is in condition for allowance. Should the Examiner have any remaining concerns, which might prevent the prompt allowance of the application, the Examiner is respectfully invited to contact the undersigned at the telephone number appearing below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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Dated: June 5, 2007

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